In the Abstract

Please amend the ABSTRACT OF THE DISCLOSURE of this application as follows:

--A processor ~~(50)~~ having a changeable architected state. The processor includes an instruction memory ~~(52)~~ for storing instructions. The processor also includes an instruction pipeline, where an instruction which passes entirely through the pipeline alters the architected state. Further, the pipeline comprises circuitry for fetching ~~(58aa)~~ instructions from the instruction memory into the pipeline. The processor also includes circuitry for storing an annul code ~~(46)~~ corresponding to instructions in the pipeline. Finally, the processor includes circuitry for preventing (FU1 through FU8) one or more selected instructions in the group from altering the architected state in response to the annul code.--

PAGE 5/26 * RCVD AT 12/9/2003 2:51:58 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:972 917 4417 * DURATI N (mm-ss):07-52